

1. (AMENDED) An integrated circuit fabrication method, comprising the steps of:

- (a.) providing a partially fabricated integrated circuit structure which has an uneven topography containing high points;
- 5 (b.) applying and curing spin-on glass, to form a first dielectric;
- (c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer;
- (d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;
- 10 (e.) performing a global etchback to substantially remove said dielectric stack from said high points of said partially fabricated structure;
- (f.) deposition of an interlevel dielectric;
- 15 (g.) etching holes in said interlevel dielectric in [predetermined] locations; and
- (h.) depositing and patterning a metallization layer to form a [desired] pattern of connections, including connections through said holes.

8. (AMENDED) An integrated circuit fabrication method, comprising the steps of:

(a.) providing a partially fabricated integrated circuit structure which has an uneven topography containing high points;

5 (b.) applying and curing spin-on glass, to form a first dielectric;

(c.) depositing silicon dioxide under vacuum conditions, to form a second dielectric layer over said first layer;

(d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers;

10 (e.) performing a global etchback to substantially remove said dielectric stack from said high points of said partially fabricated structure;

(f.) deposition of an interlevel dielectric;

15 (g.) etching holes in said interlevel dielectric in [predetermined] locations; and

(h.) depositing and patterning a metallization layer to form a [desired] pattern of connections, including connections through said holes.